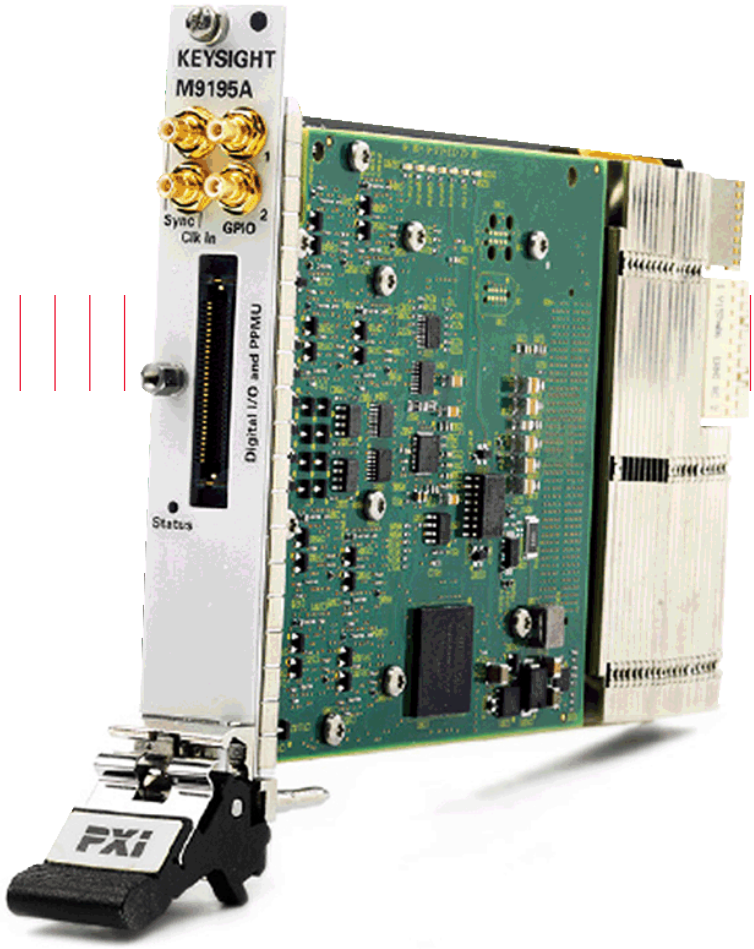
Keysight Technologies

M9195A PXIe Digital Stimulus/Response with PMU: 250 MHz, 16-channel

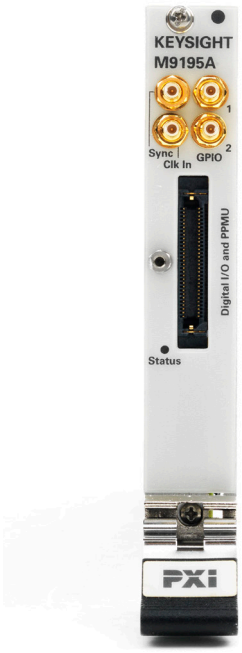
Data Sheet



KEYSIGHT TECHNOLOGIES

Overview

Experience high speed digital test capabilities at a whole new level. The Keysight Technologies, Inc. M9195A PXIe Digital Stimulus/Response (PXI DSR) module is ideal for IC design validation and production test environments. It goes beyond providing just standard capabilities. The new 16-channel, single slot PXI module introduces a high performance pattern cyclizer for powerful pattern creation and multiple drive edges per cycle for flexible edge placement. Additionally, it can support up to four independent multi-sites for quick test development and automatic response delay cable compensation. Software tools included with the M9195A allow the user to modify vector and pattern parameters without requiring the user to recompile and download tests.



Additonal ATE features include:

- High speed pattern application rate up to 250 MHz
- Per pin programming of voltage levels
- Real time compare, parametric measurement unit (PMU)
- Deep vector memory and flexible pattern sequencing

With the M9195A PXI DSR module you can easily emulate standard serial interfaces like the MIPI™ RF Front-End interface or proprietary parallel device interfaces. The test development software tools enable you to quickly create and edit waveform patterns or to import patterns created by automatic test generation applications.

Applications

- RFFE bus emulation used in PA/FEM semiconductor device verification or production test
- Wireless communication devices using parallel or serial digital control
- Automated test in product validation or manufacturing test
- Backplane emulation for device, board, or shelf testing
- Digital serial and parallel applications

Key features

- 16 bidirectional channels with per-pin programmable logic levels
- Highly flexible, per-bit timing control for fast and accurate waveform development
- Reconfigurable per-pin Parametric Measurement Unit (PMU) for each channel
- Single and multi-site configurations
- Edit patterns on-the-fly without recompiling and downloading the test
- Execute patterns in arbitrary order
- Flexible allocation of deep pattern memory per channel or per site to allocate memory where it is needed
- Channel delay adjustment to compensate for cable and fixture propagation delays
- 4 high voltage channels for flash programming or fuse test
- 4 open drain auxillary output pins for fixture relays
- Comprehensive software tool set for quick test development

M9195A hardware overview

Individual channel capability

Each of the 16 bidirectional channels provide programmable logic levels of -1.5 V to +6.5 V with up to ±75 mA of drive current. The per channel 4 quadrant parametric measurement unit (PMU) enables FVMI, FIMV, FVMV, and FIMI and FNMV modes. With the 5 PMU current ranges between ±2 µA to ±40 mA, users can make accurate leakage measurements.

For high current applications, each channel has remote sense capability to account for the voltage drop across the connecting cable. Each channel can be configured for parametric measurements, as a static digital I/O pin, or with synchronized cyclized digital data. Digital channel direction and timing can be flexibly controlled on a per digital vector basis. The cyclized data allows each pin to operate in RZ or NRZ modes. In combination with the 1 ns edge placement resolution, each pin allows for an adjustable output delay, 1 µs full range (100 ps resolution), or receive delay to enable the user to compensate for cabling propagation delays.

Multi-site capability

The PXI DSR provides a choice of a single-site configuration with 16 synchronized channels, or a multi-site configuration with 4 sets of 4 synchronized channels. In multi-site mode, each site has its own independent sequencer. This enables site independent clock operation for simultaneous testing. The multi-site capability simplifies test development. Instead of forcing the test engineer to create a single test that encompasses all for sites simultaneously, the user only needs to focus on a single device. The single device test can be easily replicated for the remaining test sites. In addition to the digital pins, each site has a high voltage drive channel and an open drain control channel for relay control.

Parametric Measurement Unit (PMU)

The PMU feature, available on each of the PXI DSR's 16 channels, enables DC current and voltage measurements. The PMUs can be independently programmed to force a voltage and measure the corresponding current, or force a current and measure the voltage. The PMU can make leakage current measurements at low current ranges or for measuring low input resistance in high current ranges. In a force voltage/measure current (FVMI) mode the PMU can measure input bias current on a single DUT pin.

Perform continuity testing of a DUT by forcing current into the pin with other DUT pins grounded while measuring the voltage at the pin (FIMV). The FNMV mode (Force Nothing, Measure Voltage) enables the PMU to be used as a scanning voltmeter. The PMU provides built-in 64 sample, 50 Hz or 60 Hz averaging to improve measurement quality by rejecting power line noise. The PMUs share a 16-bit measurement subsystem for fast accurate measurements.

Flexible digital pattern generation

With the included software tools, easily create, modify and reuse previously defined patterns. Pattern timing is controlled using up to 32 waveform tables. Within the waveform table, each of the 15 user defined vector characters is translated into one of the following hardware actions: Force High/Low (U/D), Force to previous state (P), Stop Forcing (Z), Compare High/Low (H/L), Compare to Tri-state (T), Don't Compare (X). Each vector period has two drive edges that are used when forcing a digital state and one receive edge used to compare digital data from the DUT. The edge placement resolution within a single bit period is as low a 1ns. The two drive edges enable the user to easily create a clock or other RZ formats from a single vector without requiring two vectors. The flexibility of the drive edges allow them to be changed on a per vector basis using the vector characters or by referencing a different waveform table.

The combination of the waveform tables and edge placement resolution simplifies the pattern programming. Variables and equations can be defined to allow the user to simultaneously modify timing relationships and edge placement.

Once compiled, the digital patterns are stored in the PXI DSR's on-board pattern cache. The PXI DSR executes the patterns from the cache in order to provide high test throughput. High level pattern sequencing commands allow for high level macros which can be used to define timing sets, counted and uncounted looping of pattern blocks, conditional execution based upon matching parallel or serial patterns, or wait for software trigger advance.

Advance timing capabilities

Change pattern values that have been downloaded to the cache without recompiling. Pattern values can replace either parallel vectors or serial patterns. These powerful features allow you to quickly modify patterns directly from the API. The user can create pattern templates that are used to read or write to the DUT, then provide the vector information directly from the API.

Variables can be modified at the API level without recompiling the test pattern. This allows the user to control pattern timing or levels directly from the API. These advanced capabilities useful for test applications such as a timing or voltage level shmoo.

Serial and parallel digital bus emulation

The combination of the flexible pattern timing and sequencing features, enables the PXI DSR to emulate a wide variety of standard or custom serial/parallel protocols such as SPI, I2C, and RFFE.

Comprehensive software tool set

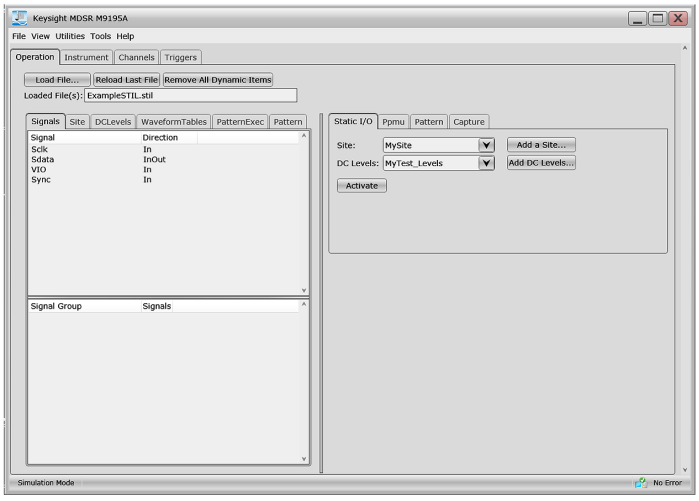
Keysight offers a choice of drivers and programming environments to configure and control the PXI DSR during test development including:

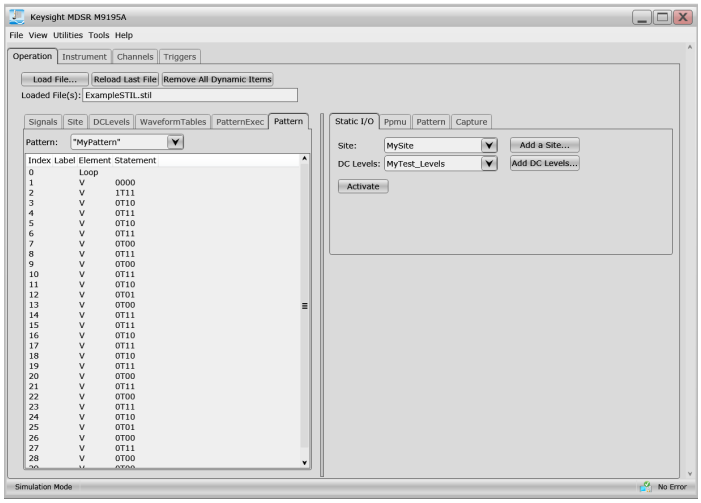
- Full featured, high-level IVI-COM, IVI-C, LabVIEW programming interfaces through drivers
- IEEE-1450/ STIL, OpenXML (Excel), or text file format for programmatically defining patterns
- The M9195A Soft Front Panel for interactive test control and debug

These test development tools can be used in powerful combinations to match the DUT's test flow and test requirements.

Soft Front Panel (SFP)

The SFP assists the user in the development and application of test patterns, allows the user to change key test execution parameters, and allows the user to validate and compensate for test fixture connectivity. During pattern development, the user interactively loads and execute STIL, XML, or bulk data tests. When loading, the tests are checked for correct syntax and the SFP generates error messages to help debug patterns. The SFP enables the user to the control various execution and response logging modes. In addition to these features, the SFP uses the same IVI interface driver calls. Each function initiated by the SFP logs an example driver call that can then be used in a regular API environment.





IVI and LabVIEW drivers

The IVI driver set can be used to fully control all aspects of test development using the DSR from assigning hardware pins to creating and executing waveform patterns using the M9195A. The drivers include high level commands for:

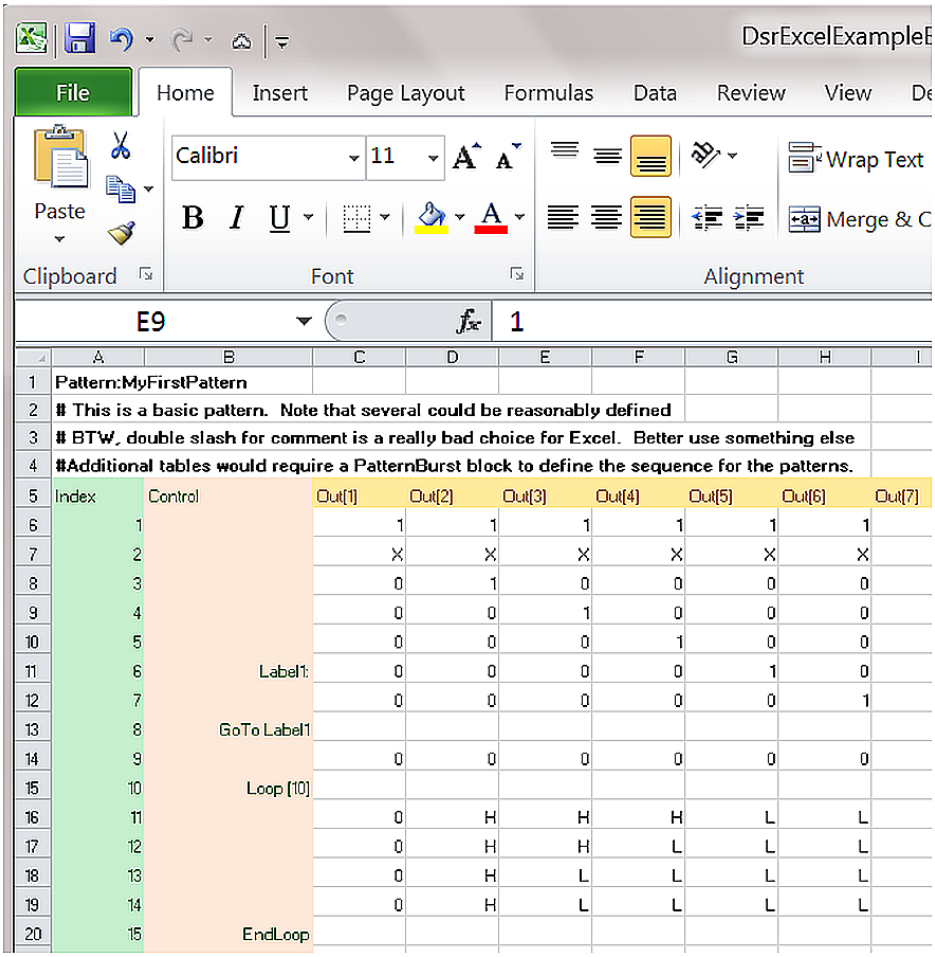
- Initial configuration including pin/channel names assignments, signal direction, grouping pins/channels to make vector definition easier.
- Setting physical layer conditions such as voltage levels, active loads
- Defining single or multisite configurations.
- Pattern definition and waveform timing.
- Pattern sequencing

Standard Test Interface Language (STIL) Support

The PXI DSR takes advantage of the Standard Test Interface language (STIL) IEEE Std 1450.0 which was designed for ATE testing. The PXI DSR can be configured using STIL commands that specify signal grouping, patterns, format, and timing information used to apply digital test vectors to a device being tested. Using a simple text editor and using the STIL format, attributes needed to generate digital patterns can quickly be created. STIL tests are easy to read and understand which simplifies test development and debug. Either the IVI API or the SFP can execute tests developed in STIL.

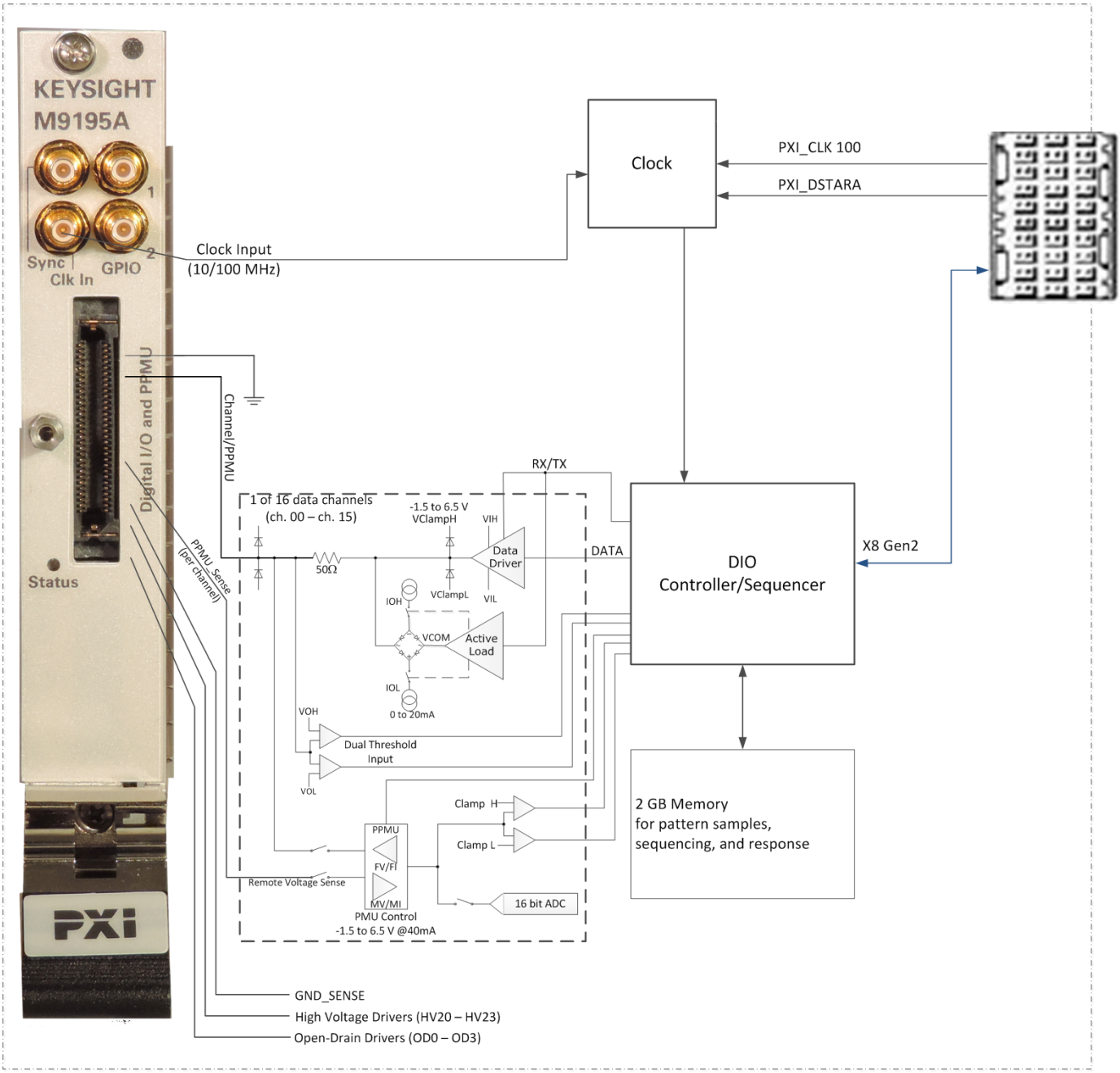
XML (.xlsx) programming interface

The XML interface allows the user to develop and debug tests in a spreadsheet form. The STIL methodology fits well with the multiple worksheet concepts provided in modern spreadsheet tools. Each worksheet matches a STIL function such as Signals, Waveform Tables, and Patterns. Digital patterns are tabular in nature and therefore fit very well into a spreadsheet. The spreadsheet provides an easy to use, flexible, and familiar interface for novice or expert users to quickly develop digital tests. All of the standard spreadsheet tools, such as equations, are available to help with pattern creation. This spreadsheet interface can be used to configure and control the M9195A channels and key features is provided as a standard development tool. Spreadsheet tests can be executed using either the SFP or associated IVI commands.



	A	B	C	D	E	F	G	H	I
1	Pattern:MyFirstPattern								
2	# This is a basic pattern. Note that several could be reasonably defined								
3	# BTW, double slash for comment is a really bad choice for Excel. Better use something else								
4	#Additional tables would require a PatternBurst block to define the sequence for the patterns.								
5	Index	Control	Out[1]	Out[2]	Out[3]	Out[4]	Out[5]	Out[6]	Out[7]
6	1		1	1	1	1	1	1	
7	2		X	X	X	X	X	X	
8	3		0	1	0	0	0	0	
9	4		0	0	1	0	0	0	
10	5		0	0	0	1	0	0	
11	6	Label1:	0	0	0	0	1	0	
12	7		0	0	0	0	0	1	
13	8	GoTo Label1							
14	9		0	0	0	0	0	0	
15	10	Loop [10]							
16	11		0	H	H	H	L	L	
17	12		0	H	H	L	L	L	
18	13		0	H	L	L	L	L	
19	14		0	H	L	L	L	L	
20	15	EndLoop							

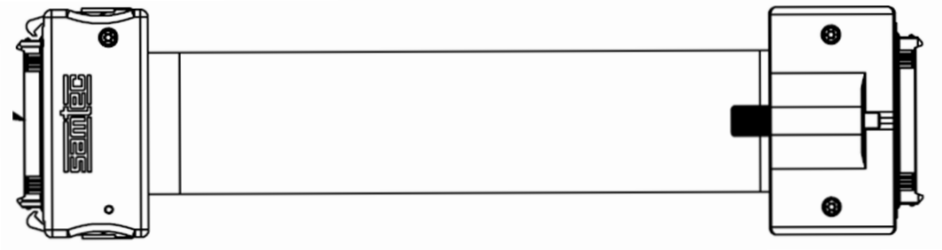
Simplified block diagram



Accessories and cables are designed for easy, accurate, and reliable digital IO connections

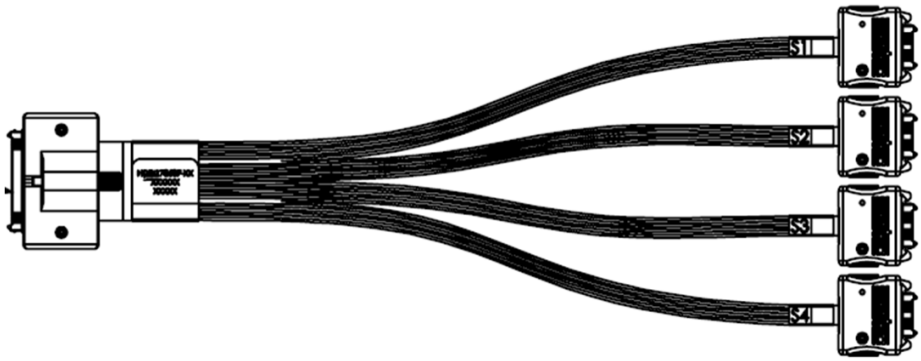
Single-site (16 channels) signal cables

- Y1246A (1 meter) or Y1247A (2 meter)
- 60 micro coax lines for 16 digital Ch, 16 PMU sense Ch, 4 high voltage Ch , and 4 open drain/grounds Ch
- Male Edge Rate™ with squeeze latches or thumb screw hood
-



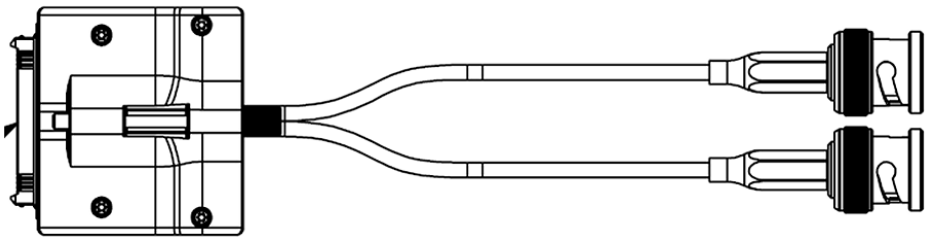
Multi-site (4 sites of 4 channels) signal cables

- 1248A (1 meter) or Y1249A (2 meter)
- 16 Ch divided into 4 independent partitions (connectors)
- Each partition contains an Edge Rate™ connector with squeeze latch, 4 digital **Ch, 4 PMU sense Ch, 1 high voltage Ch, and 1 open drain Ch**
- 4 alternate thumb screw hoods are also provided for optional use



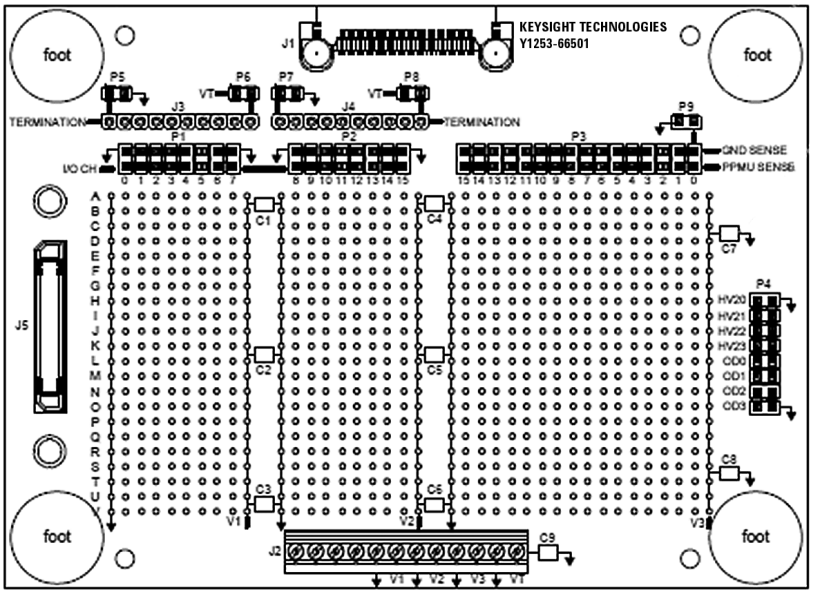
Calibration fixture

- Y1252A used to calibrate the onboard ADC and single timing from the M9195A's front panel.
- Includes hardware and instructions



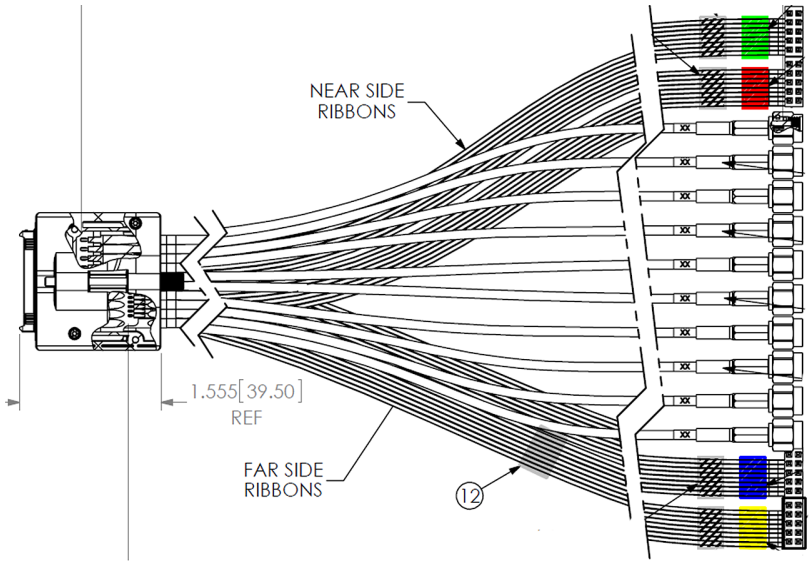
Evaluation and prototyping board

- Y1253A allows users to access individual signal pins for prototyping or debug.
- Board consists of 1 inch of signal header breakout pins, prototyping area with associated power connector, and signal termination pads.
- Offers 9in2 of bread board area, power/ground, includes headers for 16 channels, 16 PMU channels high voltage and open drain channels
- The Y1253A proto board is designed for use with the single-site, Y1246A and Y1247A, cables only.



SMA breakout cables

- Y1254A (1 meter) and Y1255A (2 meter)
- Enables user access to individual signal pins/channels for prototyping or debug
- SNA connectors plus a header for low-speed signals.
- Cables work with both the single and multi-site configurations



Definitions for specifications and characteristics

Specifications	Specifications describe the warranted performance of calibrated instruments. Specifications include guardbands to account for the expected statistical performance distribution, measurement uncertainties and changes in performance due to environmental conditions. All specifications and characteristics apply over the operating environment as outlined in the Environmental Characteristics table on page 16. Additionally, the following conditions must be met: – 30 minute warm up time with DSR software running – Calibration cycle maintained – Instrument stored in stable surrounding environment temperature between 0 to 45 °C for 2 hours before being turned on Data represented in this document are specifications if indicated by an *.
Characteristics	Characteristics describe performance that the product is expected to meet before it leaves the factory, but that is not verified in the field and is not covered by the product warranty. A characteristic includes the same guardbands as a specification. Characteristics are often referred to as typical or nominal values. Data represented in this document are characteristics unless otherwise indicated.
Best practices	To ensure proper cooling, use Keysight slot blockers (Y1212A), filler panels (Y1213A), and the air inlet module kit (Y1214A) in the chassis when there are empty slots. Keysight chassis and filler panels optimize module temperature performance. At environmental temperatures > 40 °C, chassis fans should be set to high.
Additional information	All data are measured from multiple units at room temperature and are representative of product performance within the operating temperature range unless otherwise noted. The specifications contained in this document are subject to change.

Technical specifications and characteristics

General Characteristics	
Module characteristics	
Bus interface & compatibility	PXI Express peripheral module (x1, x4, x8 PCIe specification v 2.1)
Number of data channels	16, per-channel parametric measurement unit (PPMU)
Number of sites per module	One 16 channel or four 4-channel sites
Maximum data rate for data channels	250 Mbps
Number of high voltage channels	4
Number of auxiliary open drain channels	4
Number of GPIO channels	2 [1]
Module memory	2 GB (allocated between pattern, response capture and sequence control)
Front panel connectors	
Data , open drain, HV, PPMU sense	ERCD30
Reference clock input (REF CLK IN)	SMB connector
Sync in/out (SYNC)	SMB connector [1]
GPIO 1 and GPIO 2	SMB connector [1]
Mechanical characteristics	
Dimensions (H x W x D) in mm	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connector and handle extensions
Weight	482 g

1. Reserved for future use.

Technical specifications and characteristics

DC Power Requirements		
DC supply	**Maximum**	**Typical**
DC supply current:		
+3.3 V	3.0 A	4.5 A
+12 V	2.8 A	3.0 A
Power dissipation (max)	44 W	51 W

Data Channel Characteristics		
Characteristic *** denotes warranted specification**	**Value**	**Comments**
Number of data channels	16	
Channel type	Single-ended, ground reference	
Channel impedence	50 Ω	
Direction control (In, Out, In/Out)	Per channel, per cycle (period)	
Per cycle digital states	2 drive states, 1 receive state	
Programmable drive states	Force high, force low, force terminate	Terminate state either drives active termination or is high-Z with reflection clamps
Programmable receive states	Compare high, compare low, compare three-state, compare off	Three-state: a signal level between receive high and receive low thresholds
Programmable voltage setting	Per channel	
Drive/receive voltage range	-1.5 V to +6.5 V (16-bit with 152 µV resolution)	VIH – VIL ≥ 100 mV VIL (-1.5 V to +6.4 V) VIH (-1.4 V to +6.5 V)
Drive voltage accuracy *	±25 mV (VIH & VIL) DUT centric	Maximum accuracy from ±5 ° C of AUTOCAL
Receive voltage accuracy *	±25 mV (VOH & VOL) DUT centric	Hysteresis off. Maximum accuracy from ±5 ° C of AUTOCAL
Channel output short circuit current limit	±75 mA, nominal	Maximum of 250 mA per module in combination with other channels
Channel rise time	<450 ps @ 1 V pp (programmed) <700 ps @ 3 V pp (programmed) <1300 ps @ 6 V pp (programmed)	Into 50 Ω, 20-80%, cable line compensation (CLC) setting of 3
Channel fall time	<450 ps @ 1 V pp (programmed) <700 ps @ 3 V pp (programmed) <1300 ps @ 6 V pp (programmed)	Into 50 Ω, 20-80%, cable line compensation (CLC) setting of 3
Minimum detectable voltage swing, receive	50 mV	Nominal
High impedance leakage, receive	±2 µA	Nominal. Static or dynamic digital mode
Channel power-on state	high-Z	
Receive hysteresis settings	0 mV, 50 mV, 100 mV	Typical
Channel jitter	<30 ps RMS	Typical
Channel to channel jitter	<30 ps RMS	Typical

Technical specifications and characteristics

Data Channel Characteristics **Characteristic** *** denotes warranted specification**	**Value**	**Comments**
Active termination range	-1.5 V to +6.5 V (16-bit with 152 µV resolution)	50 Ω terminated into VIT
Active termination accuracy *	±20 mV (VIT)	Maximum accuracy from ±5 ° C of AUTOCAL
Reflection clamp range	-2 V to +7 V (16-bit with 152 µV resolution)	VCH – VCL > 0.8 V VCL (-2 V to +6.2 V) VCH (-1.2 V to +7 V)
Reflection clamp accuracy	±20 mV @ 1 mA (VCH & VCL) ±200 mV @ 10 mA (VCH & VCL) ±400 mV @ 25 mA (VCH & VCL)	50 Ω source impedence into clamps. Typical accuracy from ±5 ° C of AUTOCAL neglecting source impedence voltage drop
Active load range (IOH & IOL)	0 mA to 25 mA (16-bit with 762 nA resolution)	Maximum of 250 mA per module in combination with other channels
Active load accuracy	±0.25 mA (IOH & IOL)	Typical accuracy from ±5 ° C of AUTOCAL
Commutation voltage range	-1.5 V to +6.5 V -1 V to +5.5 V	| IOL & IOH | ≤ 1 mA | IOL & IOH | ≤ 25 mA
Commutation voltage accuracy	±20 mV (VCOM)	Typical accuracy from ±5 ° C of AUTOCAL

High Voltage Channel Characteristics **Characteristic** *** denotes warranted specification**	**Value**	**Comments**
Number of high voltage channels	4	
Channel type	Single-ended, ground referenced	
Channel control	Shared with dependent data channel	HV20 shared with CH 02 HV21 shared with CH 06 HV23 shared with CH 10 HV24 shared with CH 14
Channel impedence	<10 Ω (when forcing to terminate) 50 Ω (when forcing High or Low)	Refer to user manual for HV control information
Channel power-on state	Passive 50 Ω termination	
Maximum data rate	10 MHz	Refer to user manual for HV control information
Programmable voltage range setting	Per channel	
HV drive range	0 V to +13.5 V (16-bit with 305 µV resolution)	Refer to user manual for HV control information
HV drive accuracy *	±60 mV (VHH)	Maximum accuracy from ±5 ° C of AUTOCAL
Drive voltage range	-0.1 V to +6.5 V (16-bit with 152 µV resolution)	Refer to user manual for HV control information
Drive voltage accuracy *	±30 mV (VIH & VIL)	Maximum accuracy from ±5 ° C of AUTOCAL
HV drive settling time	< 5 µs @ 13.5 V pp into 1 M Ω (1nF) < 400 µs @ 13.5 V pp into 1 M Ω (1nF)	Settled to 1% of final value
HV source/sink current per channel	±60 mA, nominal	Maximum of 250 mA per module in combination with other channels

Technical specifications and characteristics

High Voltage Channel Characteristics		
Characteristic *** denotes warranted specification**	**Value**	**Comments**
Drive rise time	<10 ps @ 1 V pp (programmed) <11 ps @ 3 V pp (programmed) <12 ps @ 6 V pp (programmed)	Into 50 Ω, 20-80%, cable line compensation (CLC) setting of 3
Drive fall time	<10 ps @ 1 V pp (programmed) <11 ps @ 3 V pp (programmed) <12 ps @ 6 V pp (programmed)	Into 50 Ω, 20-80%, cable line compensation (CLC) setting of 3
Drive source/sink current per channel	±60 mA, nominal	Maximum of 250 mA per module in combination with other channels

Open Drain Channel Characteristics		
Characteristic	**Value**	**Comments**
Number of auxiliary open drain channels	4	
Channel type	Output only, single-ended, ground referenced	
Channel terminationl	Open drain	Internal 10k Ω pull-up to +5 V
Sink current per channel	1 A max	Nominal
Channel power-on state	Off	10k Ω pull-up to +5 V

Technical specifications and characteristics

PPMU Characteristics **Characteristic** *** denotes warranted specification**	**Value**	**Comments**
Number of PPMU channels	16	
PPMU modes	Force V measure V, Force V measure I, Force I measure I, Force I measure V, Force nothing measure V	
Measurement averaging modes	None, 64 averages, 50 Hz one PLC, 60 Hz one PLC	
Force voltage range	-2 V to +6.5 V (| Current | ≤ 4 mA) -2 V to +6 V (| Current | ≤ 25 mA) -2 V to +5.75 V (| Current | ≤ 40 mA) (16-bit with 152 µV resolution)	
Force voltage accuracy *	± 10mV	Maximum accuracy from ±5 ° C of AUTOCAL. Ground sense tied to ground.
Measure voltage accuracy *	± 5mV	Maximum accuracy from ±5 ° C of AUTOCAL with one PLC averaging at sense location. Ground sense tied to ground
Force voltage settling time	< 20 µS (40 mA range) < 20 µS (1 mA range) < 30 µS (100 µA range) < 120 µS (10 µA range) < 600 µS (2 µA range)	1 V rising and falling step settled to 1% of final value into 1M Ω/ 1nF load.
Force voltage stability	Stable at all ranges into 1 µF	Larger load capacitance possible, but response limited by current slew rate.
Current range	-40 mA to + 40 mA (16-bit with 2.44 mA resolution)	Maximum of 250 mA per module in combination with other channels
	-1 mA to + 1 mA (16-bit with 61 mA resolution)	
	-100 µA to + 100 µA (16-bit with 6.1 nA resolution)	
	-10 µA to + 10 µA (16-bit with 610 pA resolution)	
	-2 µA to + 2 µA (16-bit with 122 pA resolution)	
Force current accuracy *	± 1% of range	Maximum accuracy from ±5 ° C of AUTOCAL
Measure current accuracy *	± 1% of range	Maximum accuracy from ±5 ° C of AUTOCAL with one PLC averaging
Force current settling time	Dependent on load	
Channel leakage	± 10 nA	
Remote sense	16 channels 1 GND	Ground sense should be tied to ground at measurement location for maximum accuracy.
Remote sense leakage	± 5 nA	
Force current voltage clamp range	-2 V to +6.5 V (16-bit with 152 µV resolution)	VCH > VCL VCL (-2 V to +4 V) VCH (0 V to +6.5 V)
Force current voltage clamp accuracy	± 20 mV	Typical accuracy from ±5 ° C of AUTOCAL

Technical specifications and characteristics

Timing and Trigger Specifications and Characteristics		
Channel clock		
Number of independent clock domains	1 - when configured as a single channel, 16 channel site 4 - when configured as 4, 4 channel sites	Number of independent clocks depends on the number of sites selected
Maximum clock rate	250 MHz	
Minimum clock rate	5 mHz	
Clock jitter	<30 ps RMS	
Internal reference clock		
Frequency	100 MHz	
Accuracy	±25 ppm	
Period jitter	<2 ps RMS	
Lock source settings	PXI_CLK100, PXIe-DSTARA, CLK IN	
External reference clock input (SMB front panel)		
External reference clock source	PXIe-DSTARA, CLK IN	
Input frequency	10 MHz or 100 MHz	
Input impedance (CLK IN)	50 Ω	Nominal, AC coupled
Output voltage range (CLK IN)	+1.8 V pp to + 3.3 V pp	
Lock range accuracy	±25 ppm	
Duty cycle	40 to 60%	
Channel timing (per channel)		
Waveform timing change	Per vector	
Edge placement resolution	1 ns minimum	Dependent on waveform table period
Stimulus delay resolution per test:		Dependent on waveform table period and edge placement resolution
– For EdgePlacementResolution = 1 ns and > 1 ns with ≤ 1 ns StimulusDelay	Resolution = 50 ps	
– For EdgePlacementResolution > 1 ns	Resolution = EdgePlacementResolution	
Stimulus delay range per test	Up to 250 ns x EdgePlacementResolution	
Response delay compensation resolution per test	15 ps	
Response delay compensation range per test	250 ns	
Trigger characteristics		
Trigger sources	Software (API-driven)	
Waveform characteristics		
Number of waveform tables	32	
Number of waveform characters	15 (user definable)	
Generation waveform iteration count	Once, n times, infinite	

Technical specifications and characteristics

Environmental Characteristics		
Operating and storage conditions	**Operating**	**Storage**
Temperature	0 to 45 °C	-40 to +70 °C
Humidity	Maximum 80% at 40°C (non-condensing)	
Altitude	3,000 meters, de-rate max temperature by 5 °C above 2,000 meters	
Calibration interval	1 year: return to Keysight service center or use the calibration fixture	
Mechanical		
Operating vibration	5-500 Hz: 0.21 g RMS, random 5-500 Hz: 0.5 g (0 to peak), swept sine	
Survival random vibration	5-500 Hz: 2.10 g RMS, random	
Transportation shock	40 G, 6.8 m/s, trapezoidal pulse	
End use handling shock	1.6 m/s, <3 msec duration, half-sine pulse	
Warm-up time	30 minutes	

Regulatory	
Safety	
IEC 61010-1:2001 / EN 61010-1:2001 Canada: CAN/CSA-C22.2 No. 61010-1-04 USA: ANSI/UL 61010-1:2004	
EMC	
IEC 61326-1:2012 EN 61326-1:2013	Basic EM Environments, Table 1 Criteria
IEC/EN 6100-4-2 ESD IEC/EN 61000-4-2 ESD IEC/EN 61000-4-3 RI	4 kV CD, 8 kV AD3 4 kV CD, 8 kV AD B 3 V/m: 80-1000 MHz; A1.4-2 GHz; A 1 V/m: 2-2.7 GHz
IEC/EN 61000-4-4 EFT/B IEC/EN 61000-4-5 Surge IEC/EN 61000-4-6 CI IEC/EN 61000-4-11 Dips/Inter	0.5 kV signal/control lines, 1 kV AC Mains B 0.5 kV line-line, 1 kV line-ground B 3 V, 0.15-80 MHz A 0.5 and 1 cycle @ 0% B 0.5 Sec @ 70% C
CISPR 11:2009+A1:2010 EN 55011:2009+A1:2010	Group 1 Class A (Tested in Keysight chassis)

Software information

Supported operating systems	Microsoft Windows 7 (32/64-bit)
Standard compliant drivers	IVI-COM, IVI-C, MATLAB
Supported application development environments (ADE)	VisualStudio (VB.NET, C#, C/C++), VEE, LabVIEW, LabWindows/CVI, MATLAB
Keysight IO libraries (version 16.3 or newer)	Includes: VISA libraries, Keysight Connection Expert, IO monitor
Keysight command expert	Instrument control for SCPI or IVI-COM drivers

Ordering information

Model	Description
M9195A	**PXIe Digital Stimulus/Response with PPMU: 250 MHz, 16 Ch**
M9195A-M12	Memory, 125 Mb/channel
M9195A-S04	Multi-site configuration
M9195A-SR2	Maximum clock rate, 250 MHz
Accessories and cables	
Y1246A	Single-site DSR cable: 1m
Y1247A	Single-site DSR cable: 2m
Y1248A	Multi-site DSR cable: 1m
Y1249A	Multi-site DSR cable: 2m
Y1252A	DSR Calibration fixture
Y1253A	DSR Evaluation and prototyping board
Y1254A	DSR SMA breakout cable: 1m
Y1255A	DSR SMA breakout cable: 2m

Related products

M9381A PXIe Vector Signal Generator: 1 MHz to 3 GHz or 6 GHz
M9393A PXIe Performance Vector Signal Analyzer: 9 kHz to 27 GHz
M9371A PXIe Vector Network Analyzer, 300 kHz to 6.5 GHz
M9300A PXIe Frequency Reference: 10 MHz and 100 MHz
M9018A PXIe 18-Slot Chassis
M9037A PXIe High Performance Embedded Controller

myKeysight

www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

www.pxisa.org

PCI eXtensions for Instrumentation (PXI) modular instrumentation delivers a rugged, PC-based high-performance measurement and automation system.

Three-Year Warranty

www.keysight.com/find/ThreeYearWarranty
Keysight's commitment to superior product quality and lower total cost of ownership. The only test and measurement company with three-year warranty standard on all instruments, worldwide.

Keysight Assurance Plans

www.keysight.com/find/AssurancePlans
Up to five years of protection and no budgetary surprises to ensure your instruments are operating to specification so you can rely on accurate measurements.

www.keysight.com/go/quality
Keysight Technologies, Inc.
DEKRA Certified ISO 9001:2008
Quality Management System

Keysight Channel Partners

www.keysight.com/find/channelpartners
Get the best of both worlds: Keysight's measurement expertise and product breadth, combined with channel partner convenience.

www.keysight.com/find/modular
www.keysight.com/find/m9195a

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
www.keysight.com/find/contactus

Americas

Canada	(877) 894 4414
Brazil	55 11 3351 7010
Mexico	001 800 254 2440
United States	(800) 829 4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 6375 8100

Europe & Middle East

Austria	0800 001122
Belgium	0800 58580
Finland	0800 523252
France	0805 980333
Germany	0800 6270999
Ireland	1800 832700
Israel	1 809 343051
Italy	800 599100
Luxembourg	+32 800 58580
Netherlands	0800 0233200
Russia	8800 5009286
Spain	0800 000154
Sweden	0200 882255
Switzerland	0800 805353 Opt. 1 (DE) Opt. 2 (FR) Opt. 3 (IT)
United Kingdom	0800 0260637

For other unlisted countries:
www.keysight.com/find/contactus
(BP-07-10-14)

KEYSIGHT TECHNOLOGIES

This information is subject to change without notice.
© Keysight Technologies, 2014 - 2015
Published in USA, January 27, 2015
5992-0115EN
www.keysight.com